Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A method of forming a transistor of a semiconductor device comprising:

forming an N type gate pattern and a P type gate pattern on an N type transistor area and a P type transistor area, respectively, of a semiconductor substrate;

selectively implanting N type impurities into the N type transistor area;

forming an insulation layer on the substrate including the N type gate pattern and the P type gate pattern, wherein the insulation layer has a thickness of about 160 to about 240Å;

forming a first spacer on sidewalls of the P type gate pattern by anisotropically etching a portion of the insulation layer in the P type transistor area while a portion of the insulation layer remains in the N type transistor area; and

selectively implanting P type impurities into the P type gate pattern including the first spacer and into the P type transistor area.

2. (original): The method of claim 1, wherein the N type gate pattern and the P type gate pattern include a gate oxide layer pattern and an undoped polysilicon layer pattern.

3. (currently amended): ~~The method of claim 1, further comprising~~ A method of forming a transistor of a semiconductor device comprising:

forming an N type gate pattern and a P type gate pattern on an N type transistor area and a P type transistor area, respectively, of a semiconductor substrate;

forming an oxide layer on the substrate including the N type gate pattern and the P type gate pattern to repair damage to the substrate and the gate patterns after forming the N type gate pattern and the P type gate pattern;

selectively implanting N type impurities into the N type transistor area;

forming an insulation layer on the substrate including the N type gate pattern and the P type gate pattern;

forming a first spacer on sidewalls of the P type gate pattern by anisotropically etching a portion of the insulation layer in the P type transistor area while a portion of the insulation layer remains in the N type transistor area; and

selectively implanting P type impurities into the P type gate pattern including the first spacer and into the P type transistor area.

4. (original): The method of claim 1, wherein implanting the N type impurities comprises:

forming a photoresist pattern on the substrate to selectively expose the N type transistor area;

forming an N type impurity region having a low impurity concentration and an N type conductive gate pattern by implanting the N type impurities into the N type gate pattern and into the N type transistor area using the photoresist pattern as a mask; and

removing the photoresist pattern.

5. (original): The method of claim 1, wherein the N type impurities include arsenic (As).

6. (original): The method of claim 1, wherein the insulation layer includes silicon nitride.

7. (original): The method of claim 1, wherein the insulation layer is formed at a temperature of about 700 to about 800°C.

8. (canceled).

9. (original): The method of claim 1, wherein forming the first spacer comprises:

forming a photoresist pattern on the substrate to selectively expose the P type transistor area, wherein forming the first spacer on the sidewall of the P type gate pattern by anisotropically etching the portion of the insulation layer in the P type transistor area includes using the photoresist pattern as an etching mask.

10. (original): The method of claim 9, wherein implanting the P type impurities comprises:

forming a P type impurity region having a low impurity concentration and a P type conductive gate pattern by implanting the P type impurities into the P type gate pattern and into the P type transistor area using the photoresist pattern as a mask; and

removing the second photoresist pattern.

11. (original): The method of claim 1, wherein the P type impurities include boron (B).

12. (currently amended): ~~The method of claim 1, wherein after implanting the P type impurities, further comprises:~~ A method of forming a transistor of a semiconductor device comprising:

forming an N type gate pattern and a P type gate pattern on an N type transistor area and a P type transistor area, respectively, of a semiconductor substrate;

selectively implanting N type impurities into the N type transistor area;

forming an insulation layer on the substrate including the N type gate pattern and the P type gate pattern;

forming a first spacer on sidewalls of the P type gate pattern by anisotropically etching a portion of the insulation layer in the P type transistor area while a portion of the insulation layer remains in the N type transistor area;

selectively implanting P type impurities into the P type gate pattern including the first spacer and into the P type transistor area;

selectively removing the portion of the insulation layer in the N type transistor ~~region~~ area and selectively removing the first spacer on the P type transistor region;

forming second spacers on sidewalls of the N type gate pattern and the P type gate pattern;

selectively implanting N type impurities into the N type gate pattern and into the N type transistor area; and

selectively implanting P type impurities into the P type gate pattern and into the P

type transistor area.

13. (original): The method of claim 12, wherein the insulation layer and the first spacer are selectively removed by a wet etching process.

14. (original): The method of claim 13, wherein the insulation layer and the first spacer are removed using an etching solution including phosphoric acid (H_3PO_4).

15. (original): The method of claim 12, wherein the N type impurities include phosphorus (P) or arsenic (As).

16. (original): A method of forming a transistor of a semiconductor device comprising:

forming an N type gate pattern and a P type gate pattern on an N type transistor area and a P type transistor area, respectively, of a semiconductor substrate, wherein each of the gate patterns includes a gate oxide layer pattern and an undoped polysilicon layer pattern;

forming a thermal oxidized layer on the substrate including the gate patterns to repair damage to the substrate and the gate patterns;

selectively implanting N type impurities into the N type gate patterns and into a portion of the substrate adjacent to the N type gate pattern to change the undoped polysilicon layer pattern into a conductive polysilicon layer and to form an N type impurity region having a low impurity concentration adjacent to the N type gate pattern;

forming an insulation layer on the substrate including the gate patterns;

forming a first spacer on sidewalls of the P type gate pattern by anisotropically etching a portion of the insulation layer in the P type transistor area while a portion of the insulation layer remains in the N type transistor area; and

selectively implanting P type impurities into the P type gate pattern and a portion of the substrate adjacent to the P type gate pattern to change the undoped polysilicon layer pattern into a conductive polysilicon layer pattern and to form a P type impurity region having a low impurity concentration adjacent to the P type gate pattern.

17. (original): The method of claim 16, wherein the insulation layer includes silicon nitride.

18. (original): The method of claim 16, wherein the insulation layer has a thickness of about 160 to about 240Å.

19. (original): The method of claim 16, wherein forming the first spacer comprises:

forming a photoresist pattern on the substrate to selectively expose the P type transistor area, wherein forming the first spacer on the sidewalls of the P type gate pattern by anisotropically etching the portion of the insulation layer in the P type transistor area includes using the photoresist pattern as an etching mask.

20. (original): The method of claim 19, wherein selectively implanting the P type impurities comprises:

using the photoresist pattern as a mask; and

removing the photoresist pattern.

21. (original): The method of claim 16, after forming the first spacer, further comprising:

selectively removing the portion of the insulation layer in the N type transistor area and a portion of the first spacer in the P type transistor area;

forming second spacers on sidewalls of the gate patterns;

selectively implanting N type impurities into the N type gate pattern and into the portion of the substrate adjacent to the N type gate pattern including the second spacers to form an N type impurity region having a high impurity concentration adjacent to the N type impurity region having the low impurity concentration; and

selectively implanting P type impurities into the P type gate pattern and into the portion of the substrate adjacent to the P type gate pattern having the second spacers to form a P type impurity region having a high impurity concentration adjacent to the P type impurity region having the low impurity concentration.